CPT_MPC Design Details
Jeff Andresen 4/10/2002

This document has design information for the Mini Portcard (MPC) to be fabricated by Circuits Processing Technology (CPT) Quote Number 20007850 and Fermilab P.O. number 544370. This is the prototype design with 25 tested MPCs to be delivered to Fermilab with a 10 week delivery time.

The design of the MPC from a fabrication point of view is basically the same as the design I showed CPT at my visit on 1/29/2002 with the exception that there are now only 27 holes going through the BeO layer where as there were over 60 holes before. The current design uses blind vias through the BeO layer to provide the staggered vias that were asked for to prevent a stacked through hole via through the BeO layer. The MPC is 2.000" by 1.550". There are 6 metal layers. The top three metal layers are trace layers with 3 mil traces and 3 mil clearance as minimums. The bottom 3 metal layers are split power and ground planes. There are 5 mil vias and 10 mil vias. The 27 vias going through the BeO dielectric layer are 7 mils. As the top metal layer has pads that require soldering and pads that require wire bonding and I was told that each type requires a different metal, I have Gerber file *.IN11 showing the wire bond pads and Gerber file *.IN12 showing the solder pads. The design has been done with ORCAD. Gerber files and drill files from ORCAD are being provided.

The following is the board stackup with the Gerber file extension.

Layer 1, top dielectric layer,	*.SMT	//
Layer 2, top metal layer, trace layer 1,	*.TOP	----------
Layer 3, dielectric layer 2	*.IN1	//
Layer 4, metal layer 2, trace layer 2,	*.IN2	----------
Layer 5, dielectric layer 3,	*.IN3	//
Layer 6, metal layer 3, trace layer 3,	*.IN4	----------
Layer 7, dielectric layer 4,	*.IN5	//
Layer 8, metal layer 4, ground plane	*.GND	----------
Layer 9, dielectric layer 5, BeO layer	*.IN6	//
Layer 10, metal layer 5, power plane	*.PWR	----------
Layer 11, dielectric layer 6,	*.IN7	//
Layer 12, metal layer 6, bottom plane	*.BOT	----------
Layer 13, bottom solid dielectric layer	*.SMB	//

There are the following additional files.

*.IN11 The top metal layer with only the pads that are used for wire bonding.
*.IN12 The top metal layer with only the pads that are used for soldering.

*.SST Top silkscreen layer for documentation use as text is too small for use on board.
*.TAP Drill tape files
*.ASC Netlist file from the schematic.
COMPS.TXT Components on board
CONN.TXT connections on board
*.DRD Drill drawing Gerber file
*.DTS Drill tape summary
*.LIS post processing report including aperatures
*.GTD GERBTOOL design file.

Please contact me if there are any technical questions and deliver the boards to Sergio Zimmermann or me.

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